LESSONS IN COMPOUND SEMICONDUCTOR DEVICE DEVELOPMENT

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ABSTRACT:

This paper is a mixture of personal opinion and technical fact merged to serve as a general guideline for compound semiconductor device choices. It may be construed as opinionated and contain several generalizations, but it is a result of the path taken by the author and results learned. The crucial importance of materials research in device development is the most important theme in the paper. Also, the need to minimize the complexity of device fabrication is also emphasized.

The main lesson that I learned from being part of the Eastman-group was that "Materials were the engine that drove revolutionary advances in devices." This was especially true in compound semiconductors where the lack of a compatible oxide (native or deposited) made it crucial to harness the full potential of heterostructures. This way, the devices with the potential impact of MOSFETS could be potentially invented (Note the repeated use of "potential"; a recognition that the probability of such success would still be low). To form heterostructures epitaxial techniques such as Liquid Phase Epitaxy (LPE), Molecular Bean Epitaxy (MBE), and Metalorganic Chemical Vapor Disposition (MOCVD) were sequentially invented and perfected. In my opinion, one of the great decisions of Les was to invest heavily first in MBE and subsequently in MOCVD.

Another lesson that I learned was "Do not attempt to do yourself that others can do vastly better." In these early days, the greatness of the group came substantially from the unique expertise provided by Colin Wood (MBE), Dave Woodard (Device Processing) and Gary Wicks (Characterization). With the ability to control composition, doping and thickness provided by MBE, several device advances were proposed and pursued. The driving force behind several of the projects was the attempt to harness the potential of ballistic transport in transistors. In essence, the objective was to move electrons from a source (emitter) to a drain (collector), which was placed ideally a distance less than a mean free path from the source. The goal was to minimize scattering and thereby enhance electron velocities decreasing transit times and increasing operating frequencies. This led to the next question, "Should these devices be vertical or horizontal devices?" Several groups were proposing these Extra High Frequency (EHF) devices using the Permeable Base Transistor (PBT; a vertical device at MIT Lincoln Laboratories), the Planar Doped Barrier Transistor (Cornell; vertical device), the Vertical FET (Cornell and Westinghouse), the Opposed Gate Source Transistor (OGST; Cornell and TRW, a merged vertical and lateral device) and the AlGaAs/GaAs HEMT (Cornell, GE...; a lateral device).

The seduction of vertical devices was that critical dimensions could be controlled precisely by epitaxial growth. Furthermore, techniques such as Hot Electron Launching

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using wide band gap sources to enhance electron velocities in the channel could be readily incorporated. This was indeed true. The drawbacks however turned out to be very difficult to overcome.

1. *The need to precisely define a gate on the sidewall of the conducting channel.*
   The multiple processing steps required to achieve this, primarily by planarization and deposition methods) was more difficult and progressively more expensive than improvements in linewidth and cost afforded by planar fine-line lithography.

2. *The difficulty in achieving the advantages of a recess technology.*
   A recess technology is extremely important in the non-self aligned technologies that dominate compound semiconductor FETs/HEMTs even today. The more obvious reason is the decrease in access resistance afforded by the recess for a desired threshold voltage as illustrated in figure 1.The less obvious though equally important, is the ability to design the gate to drain region such that parasitic Gunn oscillations were quenched. Such oscillations have plagued devices from GaAs MESFETs to AlInAs/GaInAs HEMTs. Figure 2 best illustrates how difficult it would be to achieve such a structure in a vertical configuration.

3. *The parasitic capacitance between the gate and drain (in a source-up device configuration).*
   This problem also plagues bipolar transistors. A gate defined via planarization and etch-back of low dielectric materials mitigate this problem as shown in figure 3. A technology such as angle evaporation is used to define a gate with the gate length a function of the pillar undercut, d_u, the evaporation angle θ, and the depth of the planarized low dielectric constant material. To remove the last variable, buried implant isolation is also a potential solution. The biggest limitation of such an approach is the lateral straggle of the implanted species (typically $\frac{1}{3} R_p$ in cubic materials in the absence of channeling). Since the doping in the channel tends to be orders of magnitude less than the $n^+ -$ region that one is trying to compensate, the implantation process can substantially raise the drain resistance of devices by compensating a fraction of the drain finger. It is easy to imagine that the entire channel can be compensated if the figures are scaled down to dimensions typical of FET channels.

So are the vertical devices really worth the bother? The answer is "Only if they offer something that lateral devices cannot." In other words in my opinion (often wrong), the de-facto choice is a lateral device. Vertical devices have been preferred in applications where

1. Maximizing current density or minimizing device area for certain on-resistance and breakdown voltage specifications is important such as in devices for power switching applications. A related advantage is in the ability to bury high field regions in a well designed vertical device which renders them less susceptible to surface phenomena.

2. When vertical devices offer functionality advantages such as
   a) Threshold uniformity afforded by bipolar transistors for critical analog operations.
   b) The ease of designing and biasing mixed-signal circuits in the zero-threshold, high g_m, f_T and f_{max} space afforded by bipolar transistors.
   c) Linearity promised by Bipolar and Static Induction Transistors (SITs).

Bipolar transistors have thrived especially in mixed signal applications because the layer structures allowed simultaneously scaling of both the vertical and lateral dimensions of the device. The problem of defining the controlling electrode (so difficult in a Vertical FET) is minor in the bipolar transistor as access to the p-type base could be achieved either through doping or etching with isolation from the emitter only an issue for self-aligned base approaches, as shown in figure 4. The use of selective etches to reveal the base accurately has enabled the thickness of the base to be scaled down to $10s$ of *nm*. The advances in high p-type doping of base materials such as GaAs, GaInAs and GaAsSb using C has allowed this scaling to occur without a penalty in sheet resistance and reduction in contact resistance. Further advances with regrown extrinsic base regions and low resistance emitter regions promise high performance, high levels of integration and reliability in the future.

My experiences guided me to primarily pursue lateral devices and concentrate on trying to incorporate the advantages of vertical devices. The first was the ability to engineer peak electric fields away from the surface in vertical devices. This led to either mimic this advantage (as in the development of the CAVET) or to mitigate electric fields on surfaces (as in FETs passivated by materials grown at low temperatures; LTG-materials or Non-Stoichiometric materials). The CAVET (Current Apertured Vertical Electron Transistor) is shown in figure 5. Here the current flows laterally along a two-dimensional electron gas channel (as in a regular HEMT) but then is collected in the bulk of the device which serves as the drain. An insulating medium prevents a direct short from the source to the drain and forms the aperture through which the drain current flows. The closest analog to this device is the DMOS in Silicon. The peak field in these devices is indeed in the bulk (as shown in the figure) and problems associated with large surface fields such as dispersion in GaN HEMTs were eliminated. In the case of LTG-GaAs passivated MESFETs the intent was to reduce surface fields by providing states close to the edge of the gate into which electrons could tunnel under high field conditions. This relieved the peaking of the field at the edge of the gate and enabled the breakdown voltage to be increased substantially. It is understandable that the nature of the states (energy level, frequency response, and density) which is controlled by the growth

conditions in MBE would impact the device performance. GaAs MESFETs with power density of over $1W/mm$ were achieved using this technique using optimal LTG-GaAs overlayers.

As a final example of the indelible link between materials advances and device enhancements it is worthwhile presenting our experience in the development of AlGaN/GaN HEMTs. In contrast to conventional materials, the wurtzite phase of GaN (the more stable and currently technologically important phase) is highly polar. Figure 7 shows the schematic of Ga-face GaN, the crystal orientation obtained by MOCVD growth. The associated crystal polarization is shown in figure 8 and the nature of polarization at an AlGaN-GaN interface is shown in figure 9. The resulting two dimensional electron gas in this system screens the difference polarization, $P(x)$, and studies have shown that the source of the electrons are surface donor states and active donors in the AlGaN layer are not required for channel formation. The lack of a lattice matched substrate requires heteroepitaxy and hence, point defects, dislocations, thermal management and surface state management all combine to determine device performance. Figure 10 charts the history of HEMT performance enhancement and links it to crucial materials advances. These are in chronological order:

1) Growing a HEMT structure with a thin GaN buffer layer on sapphire (so as to remain insulating) and demonstrating the first microwave output power from AlGaN/GaN HEMTs.

2) Improving the output power via improved thermal management, achieved by growing thick thermally conductive GaN buffer layers. This required developing a technique of growing high quality insulating buffer layers on sapphire.

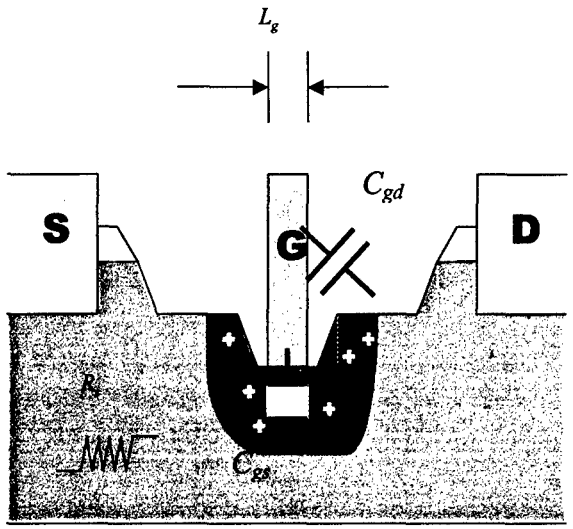
3) Next, a substantial enhancement in output power was achieved by reducing point defects close to the channel by modifying the growth conditions.

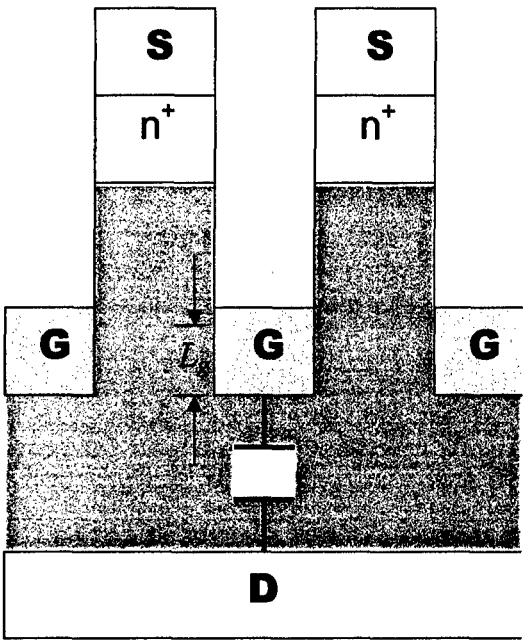
4) The last advance on sapphire substrates was achieved by applying a SiN passivating layer to the device resulting in an output power of $6.6W/mm$ on sapphire, which remains the state of the art.

5) Applying an AlN interlayer between AlGaN and GaN to reduce alloy scattering and implementing the structure on thermally conductive SiC allowed the development of devices with over $8.4W/mm$.

CONCLUSIONS:

I hope that the attempt to generalize classes of devices in this paper has not resulted in any gross misstatements. It represents my attempt to weave my experiences into a story than firm scientific fact.



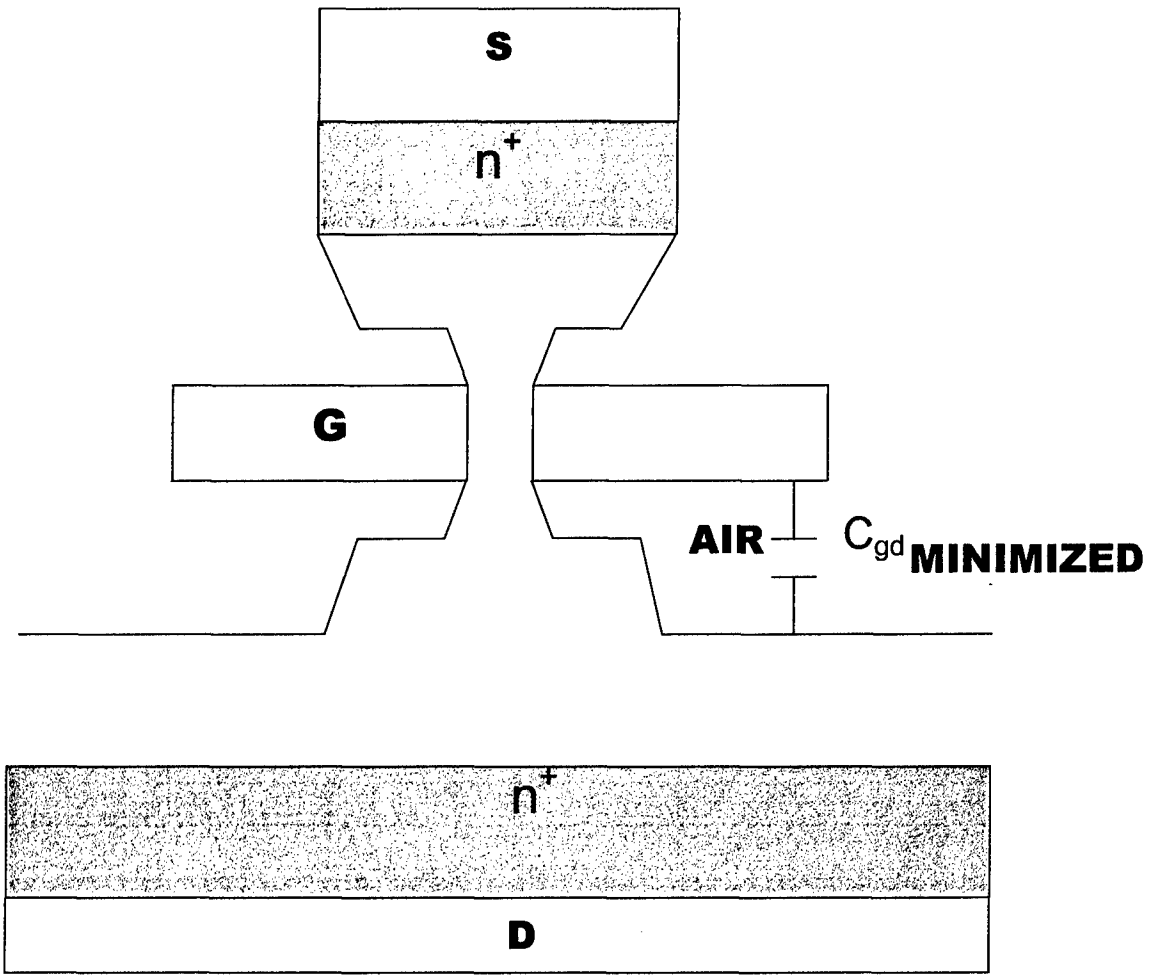


FEATURES:

- +/- GATE LENGTH Lg DETERMINES DEVICE PERFOMANCE
- + ABILITY TO RECESS DECREASES SOURCE AND DRAIN RESISTANCE AND PREVENTS GUNN-DOMAIN RELATED INSTABILITIES
- + ACTIVE DEVICE CAPACITANCE IS PARALLEL-PLATE WHEREAS PARASITIC/FEEDBACK CAPACITANCE ARE FRINGE.

- + VERTICAL DIMENSIONS ARE EASILY AND ACCURATELY CONTROLLED BY MBE/MOCVD
- + MAXIMUM FIELD CAN BE ENGINEERED TO BE IN THE BULK
- + BAND ENGINEERING IN THE DIRECTION OF CURRENT FLOW IS READILY REALIZED
- - DEFINITION OF THE GATE IS DIFFICULT
- -PARASITIC AND FEEDBACK CAPACITANCES ARE PARALLEL PLATE IN NATURE.

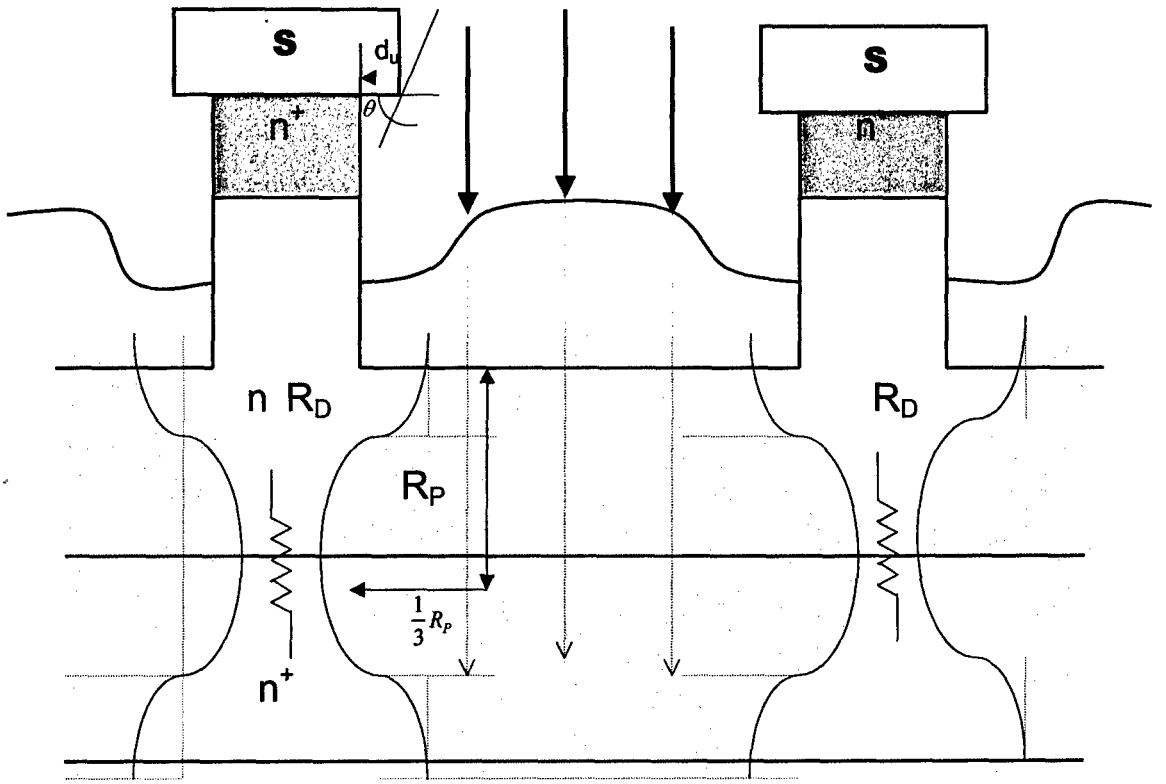
Figure 1 Comparison of lateral and vertical devices.



... A LATERAL DEVICE ROTATED
BY 90°
IS VERY HARD TO DO

Figure 2 An ideal vertical FET with the complexity of its fabrication pictorially apparent.

ISOLATION IMPLANTATION



+RELIEVES SENSITIVITY TO PLANARIZATION.
- THE LATERAL STRAGGLE OF THE IMPLANTED SPECIES CAN CAUSE AN INCREASE IN THE DRAIN RESISTANCE AND RELIEVES SENSITIVITY TO PLANARIZATION (IN EXTREME CASES CAN PINCH-OFF THE CHANNEL).

Figure 3 Schematic of method of gate definition in vertical FETs using implant isolation for reduction of parasitic gate-drain capacitance.

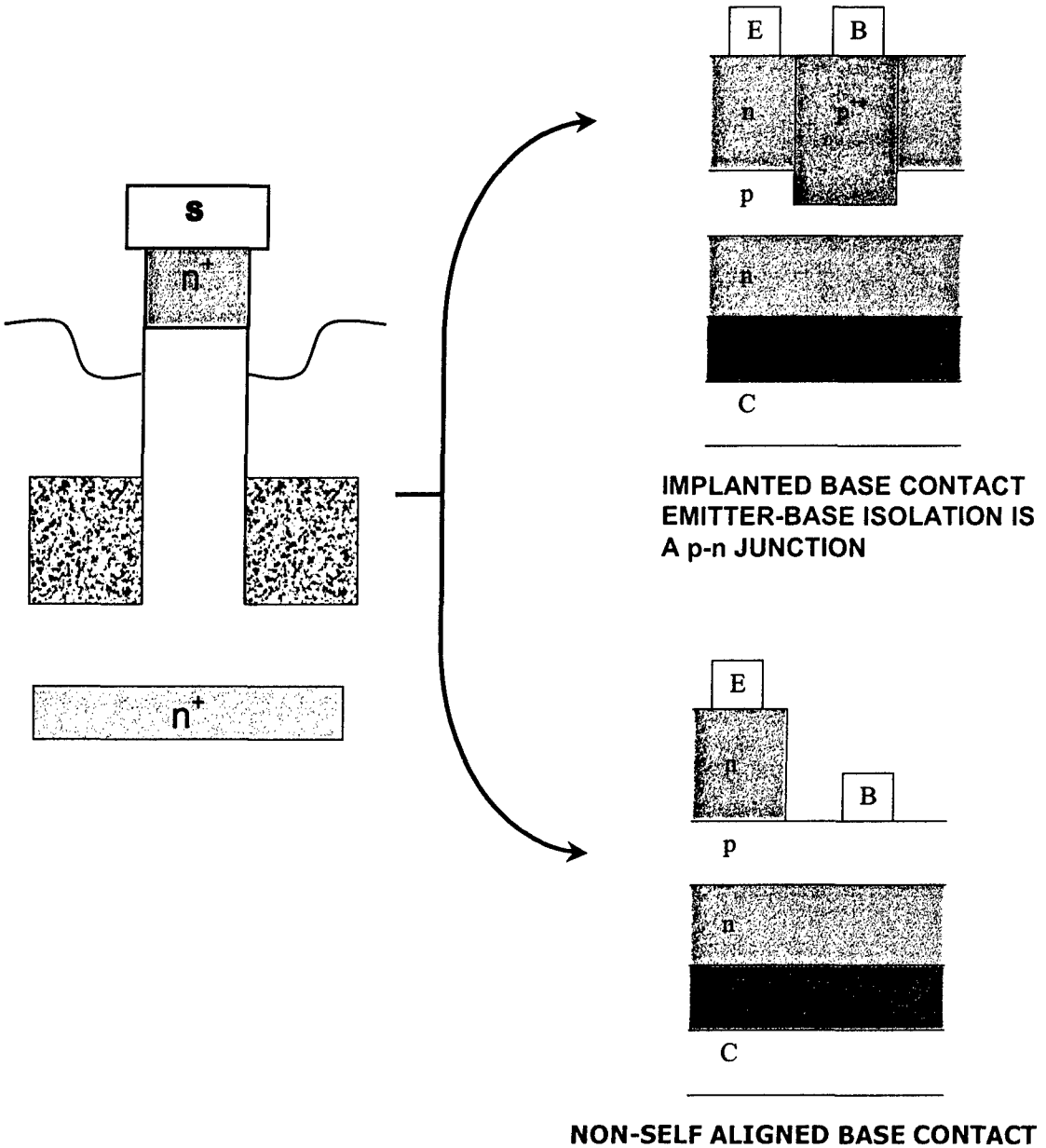
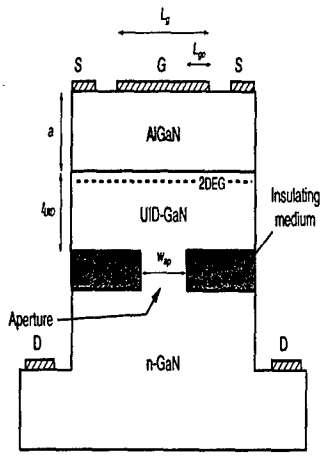
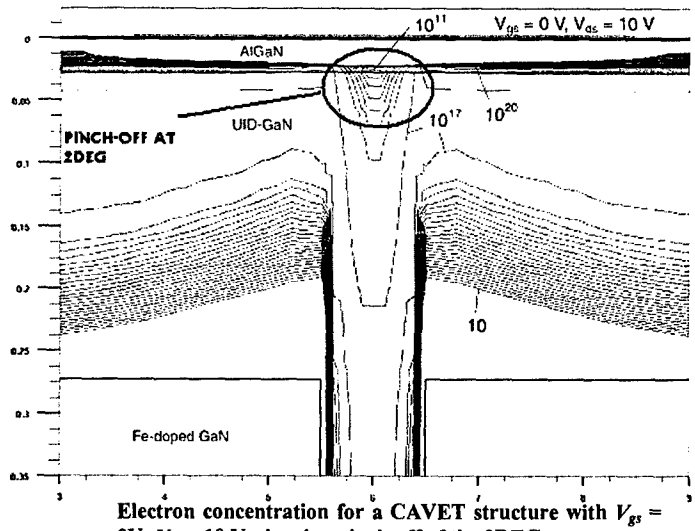


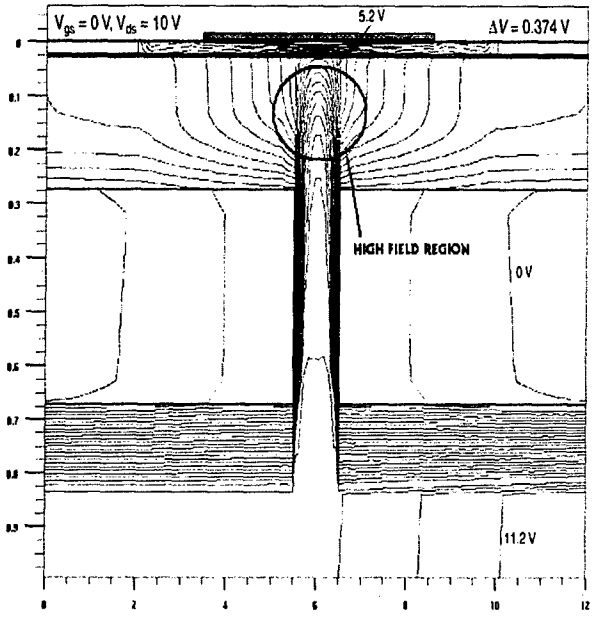
Figure 4 Advantages of bipolar transistors required for success in vertical configurations.



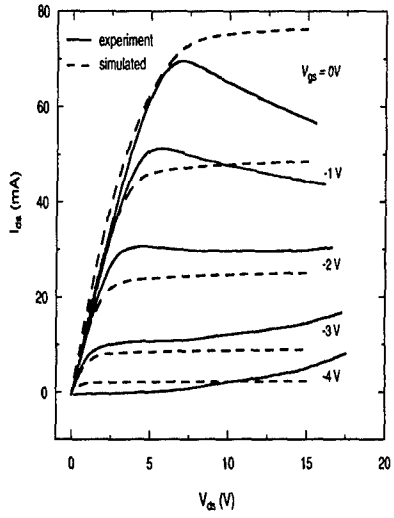
Cavet Structure



Electron concentration for a CAVET structure with V_{gs} = 0V, V_{ds} = 10 V, showing pinch-off of the 2DEG.



Equipotential lines of a CAVET structure with V_{gs} = 0V, V_{ds} = 8 V.



Experimental and simulated *I-V* characteristic of CAVET

Figure 5 The Current Apertured Vertical Electron Transistor (CAVET) demonstrating buried high field regions.

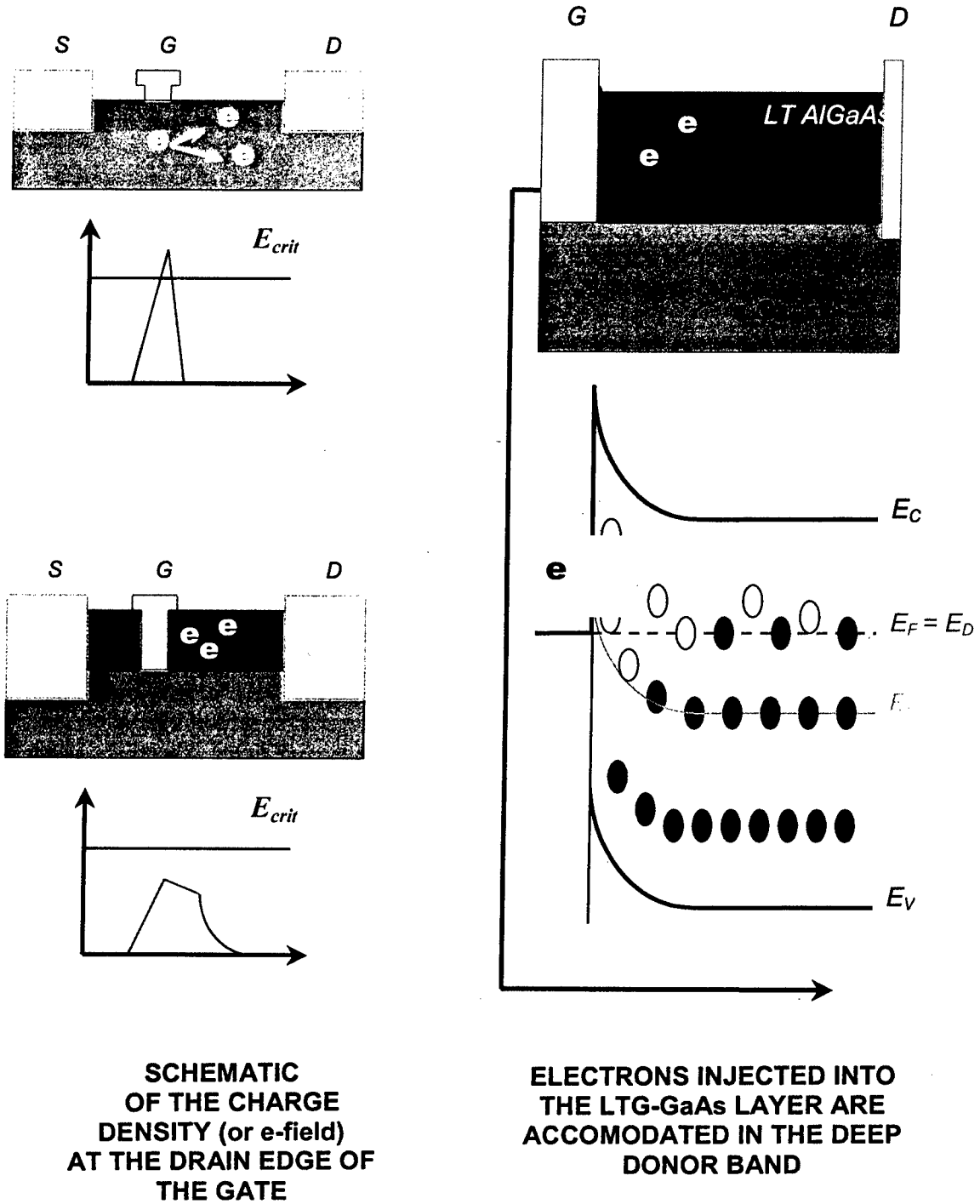


Figure 6 LTG-GaAs overlapping gate schematically illustrating surface electric field alleviation.

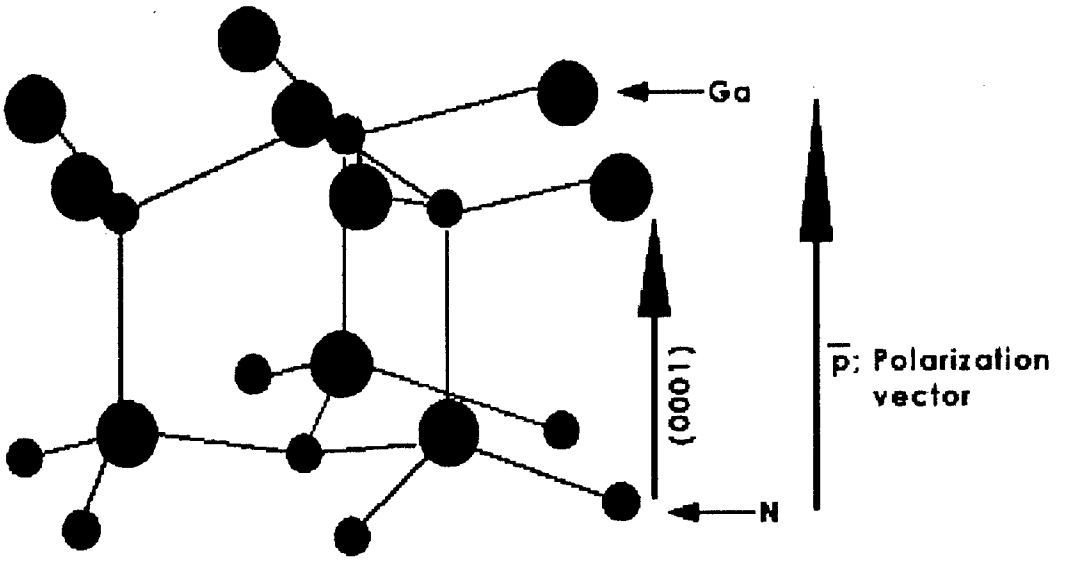
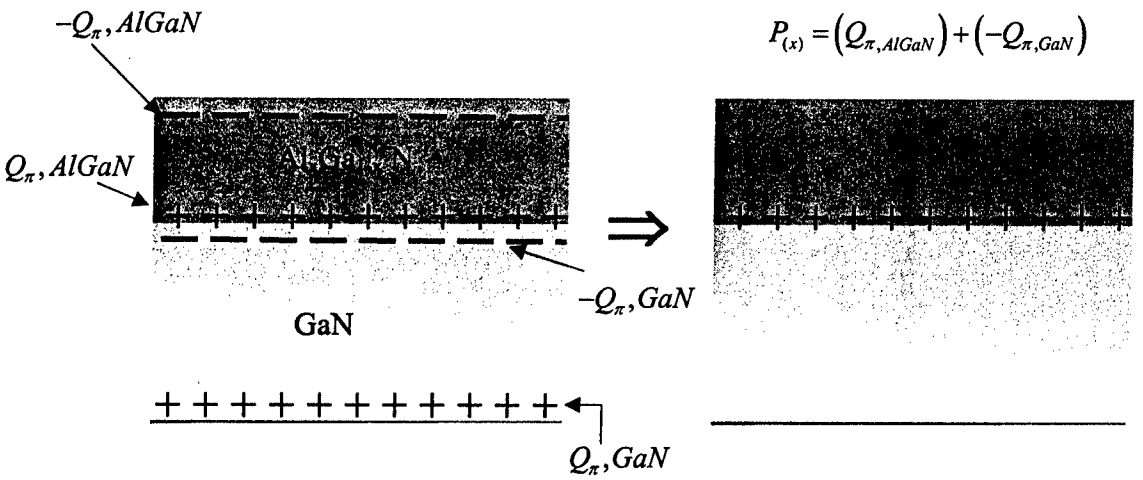


Figure 7 Ga-face GaN wurtzite crystal.



Q_π includes the contribution of spontaneous and piezo-electric contributions

Figure 8 Polarization in bulk GaN and at AlGaN/GaN interfaces.

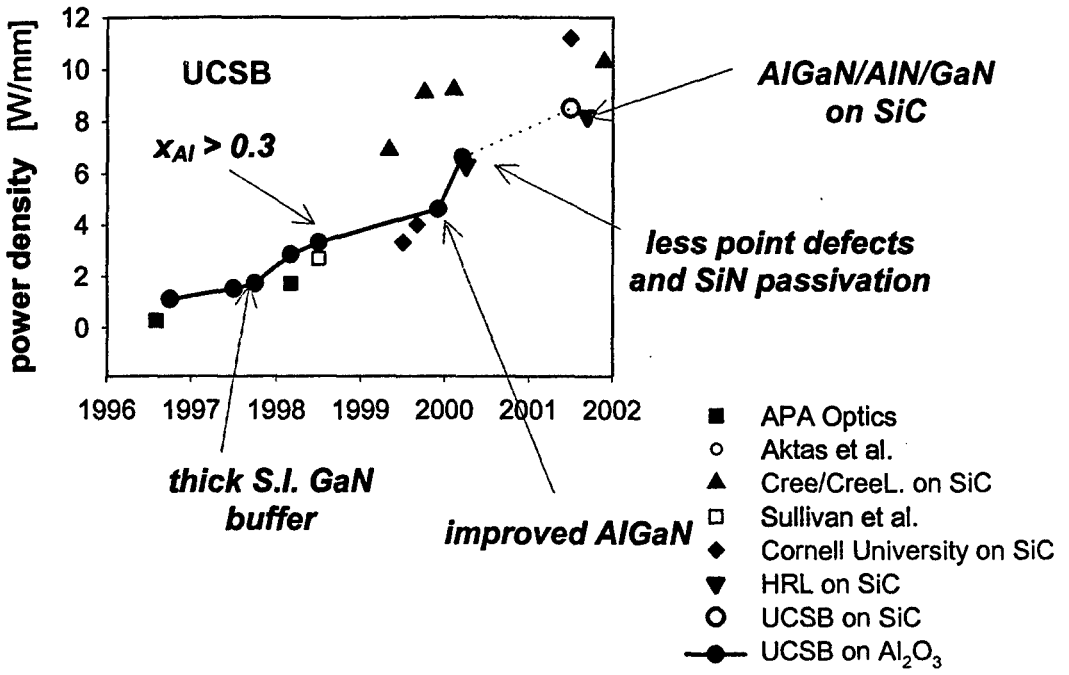


Figure 9 The direct relationship between materials improvements and AlGaN/GaN HEMT device performance as evidenced at UCSB.